REMARKS

The Examiner is thanked for the thorough examination and search of the subject.

Claims 43-74, 83, 84 and 89-102 are pending. Claims 43, 48, 54-57, 59-64, 89 and 100-102 have been currently amended. Claims 1-42, 75-82 and 85-88 have been canceled. No new matter is believed to be added herein.

Response to Claim Rejections under 35 U.S.C. 102 and 103

Applicant respectfully traverses the rejections for at least the reasons set forth below.

Response to Claims 43-63

As currently amended, independent Claim 43 is recited below:

43. A chip structure comprising:

a silicon substrate;

a resistor in said silicon substrate, wherein said resistor comprises silicon with a dopant;

a MOS device comprising a portion in said silicon substrate;

a metallization structure over said silicon substrate, wherein said metallization structure comprise a first metal layer and a second metal layer over said first metal layer;

a first dielectric layer between said first and second metal layers;

a passivation layer over said metallization structure and over said first dielectric layer, wherein a first opening in said passivation layer is over a first contact point of said metallization structure and exposes said first contact point,

and a second opening in said passivation layer is over a second contact point of said metallization structure and exposes said second contact point, wherein said first and second contact points are separated from each other by an insulating material, and wherein said passivation layer comprises silicon nitride; and

a circuit trace over said passivation layer and over said first and second contact points, wherein said first contact point is connected to said second contact point through said circuit trace, and wherein said circuit trace is connected to said resistor through said first opening.

Reconsiderations of Claims 43 and 48-55 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (U.S. Pat. No. 6,495,442) in view of Woolery et al. (U.S. Pat. No. 6,528,380), of Claims 56-62 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al. and Carichner et al. (U.S. Pat. No. 5,972,734), of Claim 63 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al. and Carichner et al. in further view of Yamada et al. (U.S. Pub. No. 2002/0047210), of Claims 44-46 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al. and Carichner et al. in further view of Leidy et al. (U.S. Pub. No. 2003/0155570), and of Claims 45 and 47 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al. and Carichner et al. in further view of Simila (U.S. Pub. No. 2003/0183332) are requested in accordance with the following remarks.

Applicant respectfully asserts that the chip structure currently claimed in Claim 43 patentably distinguishes over the citations by Lin et al. (U.S. Pat. No. 6,495,442) in view of Woolery et al. (U.S. Pat. No. 6,528,380).

The Examiner considers that Lin et al. discloses that a circuit trace (26/22/16/36/28/38) over the passivation layer, wherein said circuit trace is connected to said resistor (col. 4, lines 66-67 and col. 5, lines 1-2 describe point of contact 16 as

connected to the transistors and other devices on the surface of substrate 10, which would include the resistor. Col. 5 lines describe contact point 16 also in electrical contact with 22/36/38, which is the circuit trace. Thus, the resistor on surface of substrate is connected to the circuit trace through contact 16). ~ *See lines 17-22 on page 3, in the last Office Action mailed Jan. 3, 2008* ~

Applicant respectfully traverses the Examiner's opinion. Those skilled in the art would not consider the other devices, in Lin et al.'s disclosure, connected to a circuit trace over a passivation layer may include a resistor because no one teaches a resistor in a silicon substrate may be connected to a circuit trace over a passivation layer, as currently claimed in Claim 43.

Furthermore, both Lin et al. and Woolery et al. fail to teach, hint or suggest the claimed subject matter that a circuit trace, over a passivation layer, connecting two separate contact points exposed by two openings in the passivation layer may be connected to a resistor in a silicon substrate, as currently claimed in Claim 43.

Withdrawal of rejection under 35 U.S.C.103(a) to Claim 43 is respectfully requested.

For at least the foregoing reasons, applicant respectfully submits independent Claim 43 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 44-63 patently define over the prior art as well.

Response to Claims 64-74, 83 and 84

As currently amended, independent Claim 64 is recited below:

64. A chip structure comprising:

a silicon substrate;

a resistor in said silicon substrate, wherein said resistor comprises silicon with a dopant;

a MOS device comprising a portion in said silicon substrate;

a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer;

a dielectric layer between said first and second metal layers;

a passivation layer over said metallization structure and over said dielectric layer, wherein a first opening in said passivation layer is over a first contact point of said metallization structure and exposes said first contact point, and a second opening in said passivation layer is over a second contact point of said metallization structure and exposes said second contact point, wherein said first and second contact points are separated from each other by an insulating material, and wherein said passivation layer comprises silicon nitride; and

a circuit trace over said passivation layer and over said first and second contact points, wherein said first contact point is connected to said second contact point through said circuit trace, wherein said circuit trace is connected to said resistor through said first opening, and wherein said circuit trace comprises a titanium-containing layer and a gold layer over said titanium-containing layer.

Reconsiderations of Claims 64, 69-74 and 83 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (U.S. Pat. No. 6,495,442) in view of Woolery et al. (U.S. Pat. No. 6,528,380) and Carichner et al. (U.S. Pat. No. 5,972,734), of Claim 84 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al. and Carichner et al. in further view of Yamada et al. (U.S. Pub. No. 2002/0047210), of Claims 65-67 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al. and Carichner et al. in further view of Leidy et al. (U.S. Pub. No. 2003/0155570), and of Claims 66 and 68 rejected

under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al. and Carichner et al. in further view of Simila (U.S. Pub. No. 2003/0183332) are requested in accordance with the following remarks.

Applicant respectfully asserts that the chip structure currently claimed in Claim 64 patentably distinguishes over the citations by Lin et al. (U.S. Pat. No. 6,495,442) in view of Woolery et al. (U.S. Pat. No. 6,528,380) and Carichner et al. (U.S. Pat. No. 5,972,734).

The Examiner considers that Lin et al. discloses that a circuit trace (26/22/16/36/28/38) over the passivation layer, wherein said circuit trace is connected to said resistor (col. 4, lines 66-67 and col. 5, lines 1-2 describe point of contact 16 as connected to the transistors and other devices on the surface of substrate 10, which would include the resistor. Col. 5 lines describe contact point 16 also in electrical contact with 22/36/38, which is the circuit trace. Thus, the resistor on surface of substrate is connected to the circuit trace through contact 16). ~ *See line 18 on page 6 through line 2 on page 7, in the last Office Action mailed Jan. 3, 2008* ~

Applicant respectfully traverses the Examiner's opinion. Those skilled in the art would not consider the other devices, in Lin et al.'s disclosure, connected to a circuit trace over a passivation layer may include a resistor because no one teaches a resistor in a silicon substrate may be connected to a circuit trace over a passivation layer, as currently claimed in Claim 64.

Furthermore, all Lin et al., Woolery et al. and Carichner et al. fail to teach, hint or suggest the claimed subject matter that a circuit trace, over a passivation layer, connecting two separate contact points exposed by two openings in the passivation layer may be connected to a resistor in a silicon substrate, as currently claimed in Claim 43.

The Examiner considers that Lin also fails to disclose where said circuit trace comprises a titanium-containing layer and a gold layer over said titanium-containing layer. Carichner teaches a circuit trace (212) comprises a titanium-containing layer and a gold layer over said titanium-containing layer (col. 4, lines 41-46). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin to include the different circuit trace and metallization layers of Charichner in order to optimize the device performance under thermal stress. ~ *See lines 10-16 on page 7, in the last Office Action mailed Jan. 3, 2008* ~

Applicant respectfully traverses the Examiner's opinion because Charichner et al. fail to teach, hint or suggest that a circuit trace may comprise a titanium-containing layer and a gold layer over said titanium-containing layer, as currently claimed in Claim 64. In col. 4, lines 42-46, Charichner et al. teach that "The traces 212 are formed of any conductive material, for example copper, copper-molybdenum-copper or copper-tungsten-copper laminates, beryllium-oxide, or aluminum-nitride metallized with gold alloys or chromium, titanium or nickel", but fail to teach, hint or suggest that a circuit trace may comprise a gold layer over a titanium-containing layer. Even though the circuit trace (212) in Charichner et al.'s device could be analogous to the circuit trace 36/28/38 in Lin et al.'s device, it is believed that the claimed subject matter that a circuit trace comprises a gold layer over a titanium-containing layer, as currently claimed in Claim 64, can not be obvious over Lin et al. in view of Charichner et al. because both Lin et al. and Charichner et al. fail to teach, hint or suggest the claimed subject matter that a circuit trace comprises a gold layer over a titanium-containing layer.

Withdrawal of rejection under 35 U.S.C.103(a) to Claim 64 is respectfully requested.

For at least the foregoing reasons, applicant respectfully submits independent Claim 64 patently distinguishes over the prior art references, and should be allowed.

For at least the same reasons, dependent Claims 65-74, 83 and 84 patently define over the prior art as well.

Response to Claims 89-102

As currently amended, independent Claim 89 is recited below:

89. A chip structure comprising:

a silicon substrate;

a resistor in said silicon substrate, wherein said resistor comprises silicon with a dopant;

a MOS device comprising a portion in said silicon substrate;

a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer;

a dielectric layer between said first and second metal layers;

a passivation layer over said metallization structure and over said dielectric layer, wherein a first opening in said passivation layer is over a first contact point of said metallization structure and exposes said first contact point, and a second opening in said passivation layer is over a second contact point of said metallization structure and exposes said second contact point, wherein said first and second contact points are separated from each other by an insulating material, and wherein said passivation layer comprises silicon nitride; and

a circuit trace over said passivation layer and over said first and second contact points, wherein said first contact point is connected to said second contact point through said circuit trace, wherein said circuit trace is connected to said resistor through said first opening, and wherein said circuit trace comprises a copper layer.

Reconsiderations of Claims 89 and 94-99 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (U.S. Pat. No. 6,495,442) in view of Woolery et al. (U.S. Pat. No. 6,528,380), of Claims 100-101 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al. and Carichner et al. (U.S. Pat. No. 5,972,734), of Claim 102 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al. and Carichner et al. in further view of Yamada et al. (U.S. Pub. No. 2002/0047210), of Claims 90-92 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al. and Carichner et al. in further view of Leidy et al. (U.S. Pub. No. 2003/0155570), and of Claims 91 and 93 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al. and Carichner et al. in further view of Similа (U.S. Pub. No. 2003/0183332) are requested in accordance with the following remarks.

Applicant respectfully asserts that the chip structure currently claimed in Claim 89 patentably distinguishes over the citations by Lin et al. (U.S. Pat. No. 6,495,442) in view of Woolery et al. (U.S. Pat. No. 6,528,380).

The Examiner considers that Lin et al. discloses that a circuit trace (26/22/16/36/28/38) over the passivation layer, wherein said circuit trace is connected to said resistor (col. 4, lines 66-67 and col. 5, lines 1-2 describe point of contact 16 as connected to the transistors and other devices on the surface of substrate 10, which would include the resistor. Col. 5 lines describe contact point 16 also in electrical contact with 22/36/38, which is the circuit trace. Thus, the resistor on surface of substrate is connected to the circuit trace through contact 16). *~ See line 21 on page 4 through line 4 on page 5, in the last Office Action mailed Jan. 3, 2008 ~*

Applicant respectfully traverses the Examiner's opinion. Those skilled in the art would not consider the other devices, in Lin et al.'s disclosure, connected to a circuit trace over a passivation layer may include a resistor because no one teaches a resistor in a silicon substrate may be connected to a circuit trace over a passivation

layer, as currently claimed in Claim 89.

Furthermore, both Lin et al. and Woolery et al. fail to teach, hint or suggest the claimed subject matter that a circuit trace, over a passivation layer, connecting two separate contact points exposed by two openings in the passivation layer may be connected to a resistor in a silicon substrate, as currently claimed in Claim 89.

Withdrawal of rejection under 35 U.S.C.103(a) to Claim 89 is respectfully requested.

For at least the foregoing reasons, applicant respectfully submits independent Claim 89 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 90-102 patently define over the prior art as well.

Conclusion

Some or all Claims are believed to be in condition for Allowance, and that is so requested.

Sincerely yours,

Winston Hsu Date: 03/31/2008

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)